**EMBEDDED SYSTEMS MIDTERM EXAM**

**(10/19/2022)**

**ALEX REIGLE**

1)

module F(input a, input b, input c, input d, output OUT);

assign OUT = (b|!d) ? ((a&d)|c) : (a&(!c));

endmodule

2)

module examProblem2(input reset, input increment, output data);

reg [3:0] count;

initial

begin

count = 4'b0000;

end

always@(posedge reset or posedge increment) //async reset

begin

if(reset)

count = 4'b0000;

else if(increment)

count = count + 4'b0001;

end

F myF(.a(count[3]), .b(count[2]), .c(count[1]), .d(count[0]), .OUT(data));

endmodule

module F(input a, input b, input c, input d, output OUT);

assign OUT = (b|!d) ? ((a&d)|c) : (a&(!c));

endmodule

3)

restart -f nowave

add wave reset

add wave increment

add wave data

force reset 1 0 , 0 5

force increment 0 0, 1 1 -r 2

run 21

4)

void setup() {

pinMode(5, INPUT\_PULLUP);

pinMode(7, OUTPUT);

digitalWrite(7, HIGH);

}

void loop() {

if(digitalRead(5)==LOW){

digitalWrite(7, LOW);

}

}

5)

int count= -1;

ISR(TIMER1\_COMPA\_vect)

{

if(++count==0){ digitalWrite(6, HIGH); }

else if(count==1){ digitalWrite(6,LOW); }

else if(count==3){ count = -1; }

}

void setup() {

pinMode(6, OUTPUT);

noInterrupts();

TCCR1A = 0;

TCCR1B = 0;

OCR1A = 39; // (39.06=15624/400)

TCCR1B |= (1 << WGM12);

TCCR1B |= (1 << CS10); // 1,024 prescaler

TCCR1B |= (1 << CS12);

TIMSK1 |= (1 << OCIE1A);

interrupts();

}

void loop() {}

6)

(a) Yes FPGA lab assignments 2, 3, and 4 – used for clock input and asynchronous/synchronous behavior.

(b) a 6 bit long constant with a hexadecimal value of 21 (or 10 0001 in binary)

(c) TIMKS1 |= (1 << OCIE1A);

(d) for(int i = 0; i < 500; i++) data[i] = i%32;